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EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2186	3

DATE MAILED: 11/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/938,782	KEAYS, BRADY L.	
	Examiner	Art Unit	
	Hong C Kim	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

1. Claims 1-51 are presented for examination. This office action is in response to the application filed on 8/24/01.

Information Disclosure Statement

2. Receipt is acknowledged of information disclosure statement filed on 3/14/02, which the statement has been placed of record in the file. Information disclosed and listed on PTO 1449 was considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 33-38, 9-14, 15-19, 20, 23-25, and 42-48 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsuo et al. (Matsuo) U.S. Patent 5,923,827.

As to claim 33 , Matsuo discloses the invention as claimed. Matsuo discloses a method of

operating a Flash memory device comprising: storing an erase block management data structure in each erase block of a plurality of erase blocks of a Flash memory array (Fig. 2).

As to claim 34, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein storing the erase block management data structure further comprises storing the erase block management data structure in an at least one sector of each erase block of the plurality of erase blocks (Fig. 2).

As to claim 35, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein storing the erase block management data structure in the at least one sector of each erase block of the plurality of erase blocks further comprises storing an erase block management data value in a control section of the at least one sector (Fig. 2).

As to claim 36, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein storing the erase block management data structure in the at least one sector of each erase block of the plurality of erase blocks further comprises storing an erase block management data value in a 6 byte data field of the at least one sector (Fig. 2).

As to claim 37, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein storing the erase block management data structure further comprises storing the

erase block management data structure in a first set of sectors of each erase block of the plurality of erase blocks (Fig. 2).

As to claim 38, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein storing the erase block management data structure in a first set of sectors of each erase block of the plurality of erase blocks further comprises storing the erase block management data structure in an initial 6 sectors of the erase block (Fig. 2).

As to claim 9 , Matsuo discloses the invention as claimed. Matsuo discloses a Flash memory device comprising: a memory array containing a plurality of floating gate memory cells (flash memory reads on this limitation) divided into a plurality of erase blocks (Fig. 2), wherein each of the plurality of erase blocks is further divided into a plurality of sectors; and an erase block management data structure arranged in each erase block of the plurality of erase blocks (Fig. 2).

As to claim 10, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein each sector of the plurality of sectors has a user data section and a control data section (Fig. 2).

As to claim 11, Matsuo discloses the invention as claimed in the above. Matsuo further

discloses wherein the control data section has an erase block management data field (Fig. 2).

As to claim 12, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein the erase block management data field is a six byte data field (Fig. 2).

As to claim 13, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein a first set of sectors of the plurality of sectors contain erase block management data structures (Fig. 2).

As to claim 14, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein the first set of sectors of the plurality of sectors comprises a first six sectors of each erase block of the plurality of erase blocks (Fig. 2).

As to claim 15 , Matsuo discloses the invention as claimed. Matsuo discloses a Flash memory device comprising: a memory array containing a plurality of floating gate memory cells (Flash memory reads on this limitation) arranged in a plurality of erase blocks (Fig. 2); and an erase block management data structure arranged in each erase block of the plurality of erase blocks (Fig. 2), wherein each erase block of the plurality of erase blocks has an erase block state that is recorded in the erase block management data structure of the erase block (Fig. 2).

As to claim 16, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein the erase block state is one of "erased", "invalid", "partially filled", or "fully valid" (Figs. 3 & 5).

As to claim 17, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein the erase block state is allowed to transition directly from the "partially filled" state to the "invalid" state (Figs. 3 & 5).

As to claim 18, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein each erase block of the plurality of erase blocks contains a contiguous range of logical sector addresses (Fig. 2).

As to claim 19, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein each erase block of the plurality of erase blocks contains a single logical sector address that is repeated within the erase block (Fig.2).

As to claim 20 , Matsuo discloses the invention as claimed. Matsuo discloses a Flash memory device comprising: a memory array containing a plurality of floating gate memory cells (Flash memory reads on this limitation) arranged in a plurality of erase blocks (Fig. 2); a control circuit; and an erase block management data structure arranged in each erase block of the

plurality of erase blocks (Fig. 2).

As to claim 23, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein the control circuit manages a state of each erase block and erase block management data structure of the plurality of erase blocks (Fig. 2).

As to claim 24, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein the erase block management data structure of each individual erase block of the plurality of erase blocks contains erase block management data for the individual erase block (Fig. 2).

As to claim 25, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein each erase block and erase block management data structure of the plurality of erase blocks is written with an updated user data and an updated erase block management data with a single erase block write operation (Fig. 2).

As to claim 42 , Matsuo discloses the invention as claimed. Matsuo discloses a method of operating a Flash memory device comprising: placing an erase block management data structure in at least one sector of each erase block of a plurality of erase blocks of a Flash memory array (Fig. 2); and recording an erase block state in the erase block management data structure in the at

least one sector of each erase block of the plurality of erase blocks (Fig. 2).

As to claim 43, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein recording the erase block state in the erase block management data structure in the at least one sector of each erase block of the plurality of erase blocks further comprises recording an erase block identifier that identifies erase block format and content in the erase block management data structure in the at least one sector of each erase block of the plurality of erase blocks (Fig. 2).

As to claim 44, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein recording the erase block identifier further comprises recording an erase block identifier that identifies the erase block as containing a contiguous range of logical sector addresses (Fig. 2).

As to claim 45, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein recording the erase block identifier further comprises recording an erase block identifier that identifies the erase block as containing a single logical sector address that is repeated within the erase block (Fig. 2).

As to claim 46, Matsuo discloses the invention as claimed in the above. Matsuo further

discloses wherein recording the erase block state in the erase block management data structure in the at least one sector of each erase block of the plurality of erase blocks further comprises recording the erase block state as one of "erased", "invalid", "partially filled", or "fully valid" (Figs. 3 & 5).

As to claim 47, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein recording the erase block state further comprises allowing the erase block state to transition directly from "partially filled" to "invalid" (Fig. 3 & 5).

As to claim 48, Matsuo discloses the invention as claimed in the above. Matsuo further discloses wherein recording the erase block state in the erase block management data structure in the at least one sector of each erase block of the plurality of erase blocks further comprises recording the erase block state with an erase block operation that writes both a user data and the erase block management data in a single write operation (Fig. 2).

5. Claims 39, 41, 32, 4-6, 8, 26-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Sassa et al. (Sassa) U.S. Patent 6,144,607.

As to claim 39 , Sassa discloses the invention as claimed. Sassa discloses a method of operating a Flash memory device comprising: storing a fault tolerant erase block management data structure in a plurality of sectors of each erase block of a plurality of erase blocks of a Flash

memory array (Figs. 3s')

As to claim 41, Sassa discloses the invention as claimed in the above. Sassa further discloses wherein storing the fault tolerant erase block management data structure in the plurality of sectors of each erase block of the plurality of erase blocks further comprises storing a copy of an erase block management data field contained in a first sector of the erase block in a second sector of the erase block (Figs. 3s').

As to claim 32 , Sassa discloses the invention as claimed. Sassa discloses a method of making a Flash memory device comprising: forming a memory array containing a plurality of floating gate memory cells (Flash memory reads on this limitation) arranged in a plurality of erase blocks (Figs. 3s'); and forming an erase block management data structure in each erase block of the plurality of erase blocks (Figs. 3s').

As to claim 4 , Sassa discloses the invention as claimed. Sassa discloses a Flash memory device comprising: a memory array containing a plurality of floating gate memory cells (flash memory reads on this limitation) arranged in a plurality of erase blocks (Figs. 3s'); and an erase block management data structure arranged in each erase block of the plurality of erase blocks (Figs. 3s').

As to claim 5, Sassa discloses the invention as claimed in the above. Sassa further discloses wherein each of the plurality of erase blocks is further arranged into a plurality of sectors (Figs. 3s').

As to claim 6, Sassa discloses the invention as claimed in the above. Sassa further discloses wherein the erase block management data structure is configured in a fault tolerant data structure (Figs. 3s').

As to claim 8, Sassa discloses the invention as claimed in the above. Sassa further discloses wherein the fault tolerant data structure is a copy in a second sector of the erase block of an erase block management data field contained in a first sector of the erase block (Figs. 3s').

As to claim 26 , Sassa discloses the invention as claimed. Sassa discloses a system comprising: a host coupled to a Flash memory device (Fig. 1), wherein the Flash memory device comprises, a memory array containing a plurality of floating gate memory cells (Flash memory reads on this limitation) arranged in a plurality of erase blocks (Figs. 3s'), and an erase block management data structure arranged in each erase block of the plurality of erase blocks (Figs. 3s').

As to claim 27, Sassa discloses the invention as claimed in the above. Sassa further

discloses wherein the Flash memory device appears to the host as a rewriteable storage device (Fig.1).

As to claim 28, Sassa discloses the invention as claimed in the above. Sassa further discloses wherein the host is a processor (Fig. 1).

As to claim 29, Sassa discloses the invention as claimed in the above. Sassa further discloses wherein the host is a computer system (Fig. 1).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 40 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sassa et al. (Sassa) U.S. Patent 6,144,607 in view of Duke U.S. Patent 3,576,982.

As to claim 40, Sassa discloses the invention as claimed above. Sassa further discloses wherein storing the fault tolerant erase block management data structure in the plurality of sectors of each erase block of the plurality of erase blocks further comprises storing a component of the erase block management data structure in a first erase block management data field (Figs. 3s'),

however, Sassa does not specifically disclose a 1s complement copy of the component of the erase block management data structure in a second erase block management data field. However, it is well known in the memory art to using a 1s complement copy of the component of the erase block management data structure in a second erase block management data field for the purpose of saving backup data thereby increasing data reliability. For example, Duke discloses a 1s complement copy of the component of the erase block management data structure in a second erase block management data field (abstract).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a 1s complement copy of the component of the erase block management data structure in a second erase block management data field of Duke into the invention of Sassa for the advantages stated above.

As to claim 7, Sassa and Duke disclose the invention as claimed in the above. Sassa further discloses wherein the fault tolerant data structure is an erase block management data field (Fig. 3) and Duke further discloses a 1s complement copy of the erase block management data field (abstract).

8. Claims 22, 21, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo et al. (Matsuo) U.S. Patent 5,923,827 in view of Applicant's Admitted Prior Art (AAPA).

As to claim 22, Matsuo discloses the invention as claimed above. However, Matsuo does not specifically disclose the control circuit maps a logical address to a physical address of the plurality of erase blocks. AAPA discloses the control circuit maps a logical address to a physical address of the plurality of erase blocks (block 9) for the purpose of providing virtual mapping thereby a system addressing space appears bigger and uniform than it is.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the control circuit maps a logical address to a physical address of the plurality of erase blocks of AAPA into the invention of Matsuo for the advantages stated above.

As to claim 21, Matsuo and AAPA discloses the invention as claimed in the above. AAPA further discloses wherein the control circuit stores equivalents of the erase block management data structures of each erase block of the plurality of erase blocks into a RAM data structure (Fig. 1).

As to claim 49, Matsuo and AAPA disclose the invention as claimed in the above. AAPA further discloses comprising storing the contents of the erase block management data structures of each erase block of the plurality of erase blocks into a RAM data structure (Fig. 1).

9. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's

Admitted Prior Art (AAPA) in view of Sassa et al. (Sassa) U.S. Patent 6,144,607.

As to claim 1, AAPA discloses a Flash memory device (Fig. 1) comprising: a control circuit(fig. 1 Ref. 110); a memory array with a plurality of floating gate memory cells arranged in a plurality of erase blocks (page 2 block 4 Fig. 1 Ref. 122), wherein each erase block of the plurality of erase blocks contains 128 sectors (page 4 block 11 bottom), and each sector contains a user data section of 512 bytes (page 4 block 11 center); and a plurality of RAM control registers (Fig. 1 ref. 114). However, AAPA does not specifically disclose an erase block management data structure formed into a control data section of a first six sectors of each erase block of the plurality of erase blocks, wherein each control data section of the first six sectors contains a 6 byte erase block management data field. Sassa discloses an erase block management data structure formed into a control data section of a first six sectors of each erase block of the plurality of erase blocks, wherein each control data section of the first six sectors contains a 6 byte erase block management data field (Figs. 3s') for the purpose of enabling high speed processing (abstract).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate an erase block management data structure formed into a control data section of a first six sectors of each erase block of the plurality of erase blocks, wherein each control data section of the first six sectors contains a 6 byte erase block management data field of Sassa into the invention of AAPA for the advantages stated above.

As to claim 3, AAPA and Sassa disclose the invention as claimed in the above. Sassa further discloses wherein the first six sectors of each erase block of the plurality of erase blocks are arranged into 3 groups of 2 sector pairs, wherein both sectors of each 2 sector pair contains a complete copy of a erase block management data stored in the 2 sector pair (Figs. 3s').

10. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Sassa et al. (Sassa) U.S. Patent 6,144,607 and further in view of Duke U.S. Patent 3,576,982.

As to claim 2, AAPA and Sassa disclose the invention as claimed above. However, neither AAPA nor Sassa specifically disclose erase block management data field contain a 1s complement converted copy of the erase block management data of the first 3 bytes.
Duke discloses erase block management data field contain a 1s complement converted copy of the erase block management data of the first 3 bytes (abstract) for the purpose of saving backup data thereby increasing data reliability.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate erase block management data field contain a 1s complement converted copy of the erase block management data of the first 3 bytes of Duke into the combined invention of AAPA and Sassa for the advantages stated above.

11. Claims 50-51 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Sassa et al. (Sassa) U.S. Patent 6,144,607 in view of Applicant's Admitted Prior Art (AAPA).

As to claim 50, Sassa discloses the invention as claimed above. However, Sassa does not specifically disclose the control circuit maps a logical address to a physical address of the plurality of erase blocks. AAPA discloses the control circuit maps a logical address to a physical address of the plurality of erase blocks (block 9) for the purpose of providing virtual mapping thereby a system addressing space appears bigger and uniform than it is.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the control circuit maps a logical address to a physical address of the plurality of erase blocks of AAPA into the invention of Matsuo for the advantages stated above.

As to claim 51, Sassa and AAPA disclose the invention as claimed above. Sassa further discloses managing a state of each erase block and erase block management data structure (Figs. 3s').

As to claim 30, Sassa and AAPA disclose the invention as claimed in the above. AAPA further discloses wherein an interface to the Flash memory device is compatible with a mass storage device (block 6).

As to claim 31, Sassa and AAPA disclose the invention as claimed in the above. AAPA further discloses wherein an interface to the Flash memory device is a PCMCIA-ATA compatible

interface (block 7).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

13. a shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

14. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

15. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

16. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matt Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

17. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to TC-2100:
Official (703) 872-9306, New as of 8/4/2003
After-Final (703) 746-7238
Official (703) 746-7239 (for formal communications intended for entry)

Non-Official/Draft (703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Primary Patent Examiner
November 11, 2003